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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/535,233	03/24/2000	Masaya Kadono	SEL 171	1670

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EXAMINER
COLEMAN, WILLIAM D

ART UNIT	PAPER NUMBER
2823	

DATE MAILED: 03/26/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/535,233	Applicant(s) KADONO ET AL.	
	Examiner W. David Coleman	Art Unit 2823	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 January 2001* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☐ Claim(s) _____ is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *11-30* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Response to Arguments

1. Applicant's contend that amending claims 11, 15 and 23 to include a semiconductor film and a gate insulating film will overcome the rejection mailed August 29, 2001.

2. However, because the references teach forming semiconductor films (i.e., using silicon) and gate insulating films (one of the foundation principles in semiconductor technology) as claimed, the Applicants have not overcome the rejection.

3. It is noted that Applicant's did not traverse the rejection of claims 19-23.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 11-14 are rejected under 35 U.S.C. 102(b) as being anticipated by Belscher et al., U.S. Patent 5,792,327.

6. Pertaining to claim 11, Belscher discloses a semiconductor process as claimed. Belscher teaches a method of manufacturing a semiconductor device, comprising steps of:

forming a semiconductor film (amorphous silicon (column 1, line 24)),

removing a contaminating impurity from the surface of the first film; and forming a gate insulating film (inherent) in contact with the semiconductor film from the surface of which the contaminating impurity (alkali metal ions (column 2, lines 66-67)) has been removed.

7. Pertaining to claims 12 and 13, Belscher discloses at least one element selected from periodic table group 1 elements or periodic table group 2 elements. Please note that since Belscher teaches the removal of alkali earth metals (column 3, line 67), it is inherent that alkali earth metals are from at least periodic table group 1 or periodic table group 2.

8. Pertaining to claim 14, Belscher teaches a method wherein the contaminating impurity is removed by an acidic solution containing fluorine (hydrofluoric acid) (column 3, line 26).

Claim Rejections - 35 USC § 103

9. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

10. Claims 15-30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kobayashi et al., U.S. Patent 5,102,813 in view of Mautz et al., U.S. Patent 5,476,816.

11. Pertaining to claim 15, Kobayashi discloses a semiconductor process substantially as claimed. See **FIGS. 7A-7C**, where Kobayashi teaches a method of manufacturing a semiconductor device, comprising the steps of:

forming at least one semiconductor island **21** (also see column 4, lines 53-54) over a substrate **22**;

forming a gate insulating film **23** over said semiconductor island. However, Kobayashi fails to teach spinning the substrate by using a spinning apparatus; contacting an etching solution to a surface of said semiconductor island and scattering the etching solution during said spinning,

thereby contaminating impurities are removed from the surface. Mautz teaches a step of spinning the substrate by using a spinning apparatus, see **FIGS. 2-8** of Mautz, (the substrate spins at a speed in a range of 25-100 revolutions per minute) (column 6, lines 65-67),

contacting an etchant solution (ammonium fluoride) (column 5, line 32) to a surface of said semiconductor island and scattering the etching solution during said spinning, thereby contaminating impurities are removed from the surface (i.e., semiconductor device islands) (column 5, lines 3-4). The first interlevel insulating layer **28** is exposed to a fluoride-containing etching solution,

forming an insulating film **71** (as seen in **FIG. 7** of Mautz) over said semiconductor island.

In view of Mautz it would have been obvious to one of ordinary skill in the art to incorporate a spin etching step in the Kobayashi process because the etch removes at least 75 percent of the mobile ions within the insulating layer (abstract, lines 7-8).

Pertaining to claims 16, 20, 24 and 28, Kobayashi teaches an etching solution consisting of hydrogen fluoride (column 2, line 54).

12. Pertaining to claims 17, 18, 21, 22, 25, 26, 29 and 30, Kobayashi fails to teach wherein the contaminating impurity is at least one element selected from periodic table group 1 elements or periodic table group 2 elements, where the contaminating impurity is at least one element selected from the group consisting of sodium, lithium, potassium, calcium and magnesium. Mautz teaches a process step wherein the contaminating impurities are at least from periodic table group 1 or periodic table group 2 consisting of sodium, lithium, potassium, calcium and magnesium.

In view of Mautz it would have been obvious to one of ordinary skill in the art to remove the claimed contaminating impurities because mobile ions, such as sodium, lithium, potassium, calcium and magnesium degrade device reliability (column 1, lines 15-17).

13. Pertaining to claims 19, 23 and 27, Kobayashi discloses a semiconductor process substantially as claimed. See **FIGS. 7A-7C**, where Kobayashi teaches a method of manufacturing a semiconductor device, comprising the steps of:

forming a gate insulating film 23 and a semiconductor film **24** over a substrate **22**;

crystallizing said semiconductor film (deposit an amorphous silicon layer at 550^0 C., after which annealing is executed at 630^0 C) (column 2, lines 45-50);

forming gate wirings **29** (**FIG. 7C** of Kobayashi) over a substrate

forming an insulating film **28** over said semiconductor island. However, Kobayashi fails to teach spinning the substrate by using a spinning apparatus; contacting an etching solution to a surface of said semiconductor island and scattering the etching solution during said spinning, thereby contaminating impurities are removed from the surface. Mautz teaches a step of spinning the substrate by using a spinning apparatus, see **FIGS. 2-8** of Mautz, (the substrate spins at a speed in a range of 25-100 revolutions per minute) (column 6, lines 65-67),

contacting an etchant solution (ammonium fluoride) (column 5, line 32) to a surface of said semiconductor island and scattering the etching solution during said spinning, thereby contaminating impurities are removed from the surface (i.e., semiconductor device islands) (column 5, lines 3-4). The first interlevel insulating layer **28** is exposed to a fluoride-containing etching solution,

forming an insulating film **71** (as seen in **FIG. 7** of Mautz) over said semiconductor island.

In view of Mautz it would have been obvious to one of ordinary skill in the art to incorporate a spin etching step in the Kobayashi process because the etch removes at least 75 percent of the mobile ions within the insulating layer (abstract, lines 7-8).

Conclusion

14. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

15. Any inquiry concerning this communication or earlier communications from the examiner should be directed to W. David Coleman whose telephone number is 703-305-0004. The examiner can normally be reached on 9:00 AM-5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael M. Fahmy can be reached on 703-308-4918. The fax phone numbers for the

organization where this application or proceeding is assigned are 703-308-7722 for regular communications and 703-308-7721 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

WDC
March 16, 2002